wherein the system bridge controller performs format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and between the CPU and one or more of the plurality of peripheral devices,

wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.

42. The system of claim 41 wherein the MPEG Transport processor, the MPEG video decoder, the means for displaying the video and the system bridge controller are integrated on an integrated circuit chip.

45. (New) The system of claim 1, wherein the system bridge controller supports delayed read and retry of reads by external masters, thereby allowing higher I/O bus throughput.

46. (New) The system of claim 1, wherein the system bridge controller supports retry cycles when it is a master.

47. (New) The method of claim 22, wherein the system bridge controller supports delayed read and retry of reads by external masters, thereby allowing higher I/O bus throughput.

48. (New) The method of claim 22, wherein the system bridge controller supports retry cycles when it is a master.

REMARKS

Claims 1-3, 5-39, 41-42 and 45-48 are pending in the present application, of which claims 1, 22 and 41 are independent. Claims 4, 40 and 43-44 have been canceled, and new claims 45-48 have been added. Applicants respectfully request reconsideration and allowance of claims 1-3, 5-39, 41-42 and 45-48.

The Examiner has rejected claims 1-44 under U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,982,459 to Fandrianto et al. ("Fandrianto").

The Examiner agrees that "Fandrianto fails to specifically disclose '...a north bridge function...wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.'" However, the Examiner combines Fandrianto with page 2, lines 9-15 ("Video and graphics systems are typically used in television control electronics, such as set top boxes, integrated digital TVs, and home network computers. When conventional video and graphics system on integrated circuit chips are used with a host CPU in the television control electronics, a separate bridge controller, which is also referred to as a 'north bridge,' is typically used to couple the host CPU to peripheral devices") of the present application to reject the claims of the present application.

Applicants respectfully submit that this combination of references to reject the claims of the present application is improper because applicants do not believe there is any teaching, suggestion or motivation to integrate the "north bridge" function onto an integrated circuit chip with a video and graphics system. In fact, one of the problems with the prior art is given by applicants on page 183, line 35 through page 184, line 2 of the present application as "Use of the bridge controller increases number of chips in the system and introduces another potential source of system failure." This problem and the solution to the problem is not in the background section; rather, a solution provided by the present invention is a novel and unobvious way of reducing the number of chips and to not introduce another potential source of system failure.

The case law supports the conclusion that the fact that references can be combined or modified is not sufficient to establish prima facie obviousness. For example, the Federal Circuit has held that "The mere fact that the prior art could be so modified would not

have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Mills*, 916 F.2d 680, 682, 16 USQP2d 1430, 1432 (Fed. Cir. 1990).

In *In re Mills*, claims were directed to an apparatus for producing an aerated cementitious composition by drawing air into the cementitious composition by driving the output pump at a capacity greater than the feed rate. The prior art reference taught that the feed means can be run at a variable speed, however the court found that this does not require that the output pump be run at the claimed speed so that air is drawn into the mixing chamber and is entrained in the ingredients during operation. According to the court, although a prior art device may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so. *In re Mills*, 916 F.2d at 682, 16 USPQ2d at 1432.

Similarly in the present instance, even if the integrated multimedia communications processor and codec of Fandrianto were capable of being modified to incorporate the "north bridge" function, there must be a suggestion or motivation in the references to do so. Applicants respectfully submit that there is no such suggestion or motivation in Fandrianto or in the cited passage of the background section. Therefore, applicants respectfully submit that the rejection of claims 1-3, 5-39, 41-42 and 45-48 on obviousness grounds was not proper.

The conclusion that such combination is not obvious finds a further support when considering the prior art made of record and not relied upon, which the Examiner considers pertinent to the present application. These references were cited by the Examiner on Form PTO-892 at the time of mailing the Office Action mailed July 5, 2001. These reference are U.S. Patent No. 5,640,543 to Farrell et al. ("Farrell"), U.S. Patent No. 5,790,795 to Hough ("Hough") and U.S. Patent No. 6,018,803 to Kardach ("Kardach").

For example, FIG. 1 of Farrell illustrates a bridge 34 that

interfaces between CPU 38 and Hard Disk 52, CD ROM 54; FIG. 4 of Hough illustrates a system bus interface 222 that interfaces between a local processor 214 and other devices on a bus 224; and FIG. 1 of Kardach illustrates a bus bridge & memory controller 108 that interfaces between a processor 100 and other devices on a peripheral bus 110. Since none of these references appears to teach or suggest that a "north bridge" function can be integrated with a video and graphics system on an integrated circuit chip, applicants respectfully submit that these references provide a further evidence that it is not at all obvious to integrate the "north bridge" function with a video and graphics system on an integrated circuit chip.

Claim 1 recites, in relevant portion, "a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices, wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip."

Since neither of the cited passage in the background section and Fandrianto teaches, suggests or provides any motivation to combine the references to practice a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices, wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip, applicants respectfully request that the rejection to claim 1 be withdrawn and that claim 1 be allowed.

Since claims 2-3 and 5-21 depend, directly or indirectly, from claim 1, they incorporate all the terms and limitations of claim 1 in addition to other limitations, which together patentably distinguish them from the cited references. Therefore, applicants respectfully request that the rejection to claims 2-3 and 5-21 be withdrawn and that they be allowed.

Claim 22 recites, in relevant portion, "coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip, wherein the

integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video, and wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip."

Since neither of the cited passage in the background section and Fandrianto teaches, suggests or provides any motivation to combine the references to practice coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip, wherein the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video, and wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip, applicants respectfully request that the rejection to claim 22 be withdrawn and that claim 22 be allowed.

Since claims 23-40 depend, directly or indirectly, from claim 22, they incorporate all the terms and limitations of claim 22 in addition to other limitations, which together patentably distinguish them from the cited references. Therefore, applicants respectfully request that the rejection to claims 23-39 be withdrawn and that they be allowed.

Claim 41 recites, in relevant portion, "a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices . . . wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip."

Since neither of the cited passage in the background section and Fandrianto teaches, suggests or provides any motivation to combine the references to practice a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices . . . wherein the CPU and the plurality of peripheral devices are situated

externally to the integrated circuit chip, applicants respectfully request that the rejection to claim 41 be withdrawn and that claim 41 be allowed.

Since claim 42 depends from claim 41, it incorporates all the terms and limitations of claim 41 in addition to other limitations, which together patentably distinguish it from the cited references. Therefore, applicants respectfully request that the rejection to claim 42 be withdrawn and that it be allowed.

Claims 45-48 have been added. These claims find support in the specification as filed, for example, on page 186, line 31 through page 187, line 2. Since claims 45-48 depend, directly or indirectly, from claims 1 and 22, respectively, they incorporate all the terms and limitations of either claim 1 or claim 22 in addition to other limitations, which together patentably distinguish them from the cited references. Therefore, applicants respectfully request that claims 45-48 be allowed.

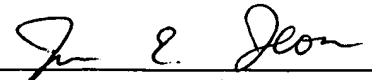
Claims 4, 40 and 43-44 have been canceled herein, and the rejection to these claims are now moot.

In view of the foregoing remarks, Applicants respectfully request allowance of claims 1-3, 5-39, 41-42 and 45-48. If the Examiner believes that a telephone conference with Applicants' attorney might expedite prosecution of the application, the Examiner is invited to call at the telephone number indicated below.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By 

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JEJ/sd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 1, lines 14-31, please replace with the following paragraph:

The present application contains subject matter related to the subject matter disclosed in U.S. patent application number 09/641,374 [————————] entitled "Video, Audio and Graphics Decode, Composite and Display System," U.S. patent application number 09/641,936 [————————] entitled "Video and Graphics System with an MPEG Video Decoder for Concurrent Multi-Row Decoding," U.S. patent application number 09/643,223 [————————] entitled "Video and Graphics System with MPEG Specific Data Transfer Commands," U.S. patent application number 09/640,870 [————————] entitled "Video and Graphics System with Video Scaling," U.S. patent application number 09/640,869 [————————] entitled "Video and Graphics System with a Data Transport Processor," U.S. patent application number 09/641,930 [————————] entitled "Video and Graphics System with a Video Transport Processor," U.S. patent application number 09/641,935 [————————] entitled "Video and Graphics System with Parallel Processing of Graphics Windows," and U.S. patent application number 09/642,510 [————————] entitled "Video and Graphics System with a Single-Port RAM [~~Used Similarly as a Dual-Port RAM~~]," all filed August 18, 2000.